

111

DIAS et al.

YOR920010401US1 (6Hz)

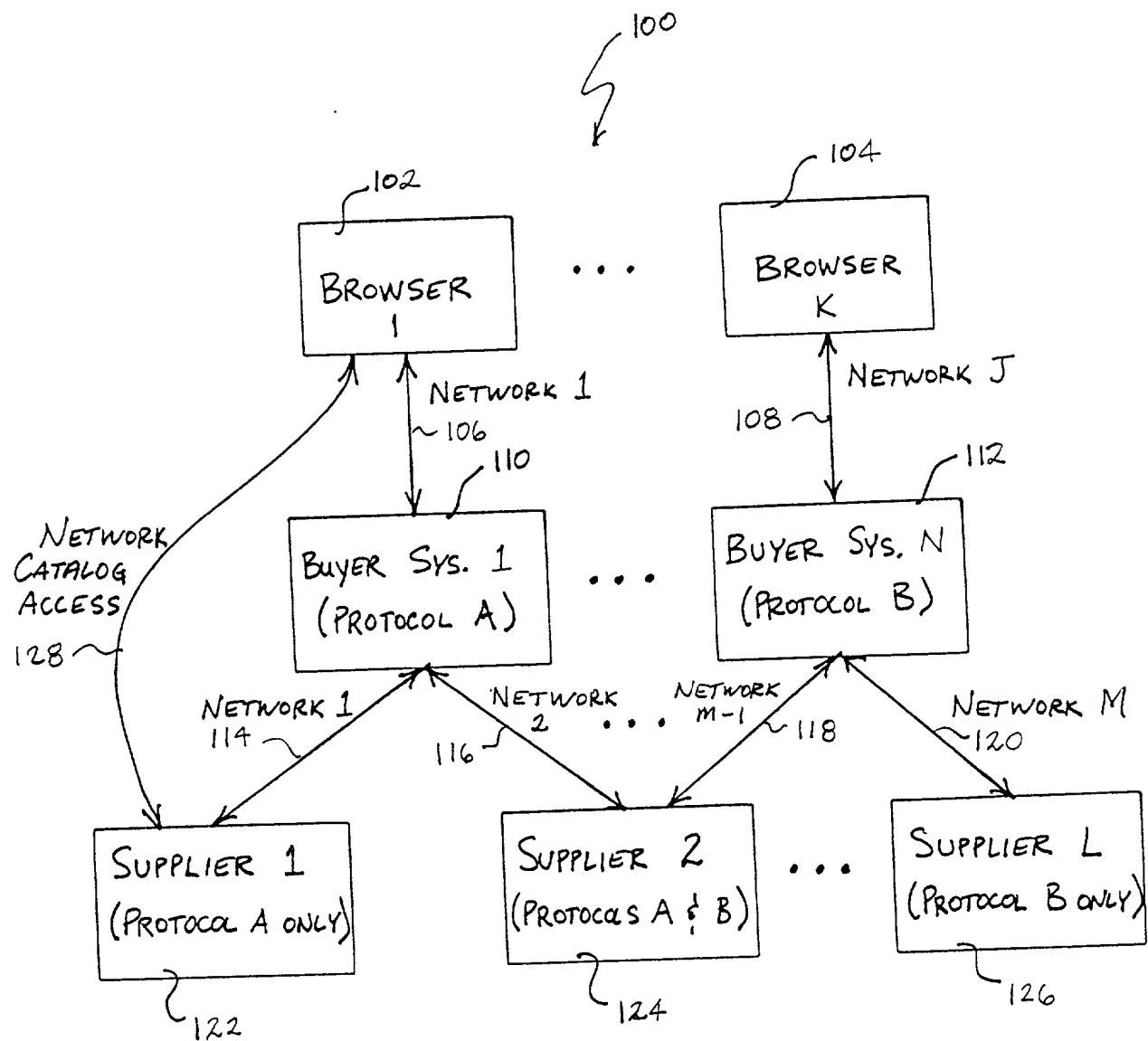


FIG. 1
(PRIOR ART)

2/11
Y0R920010401US1

PROPOSED SYSTEM ARCHITECTURE

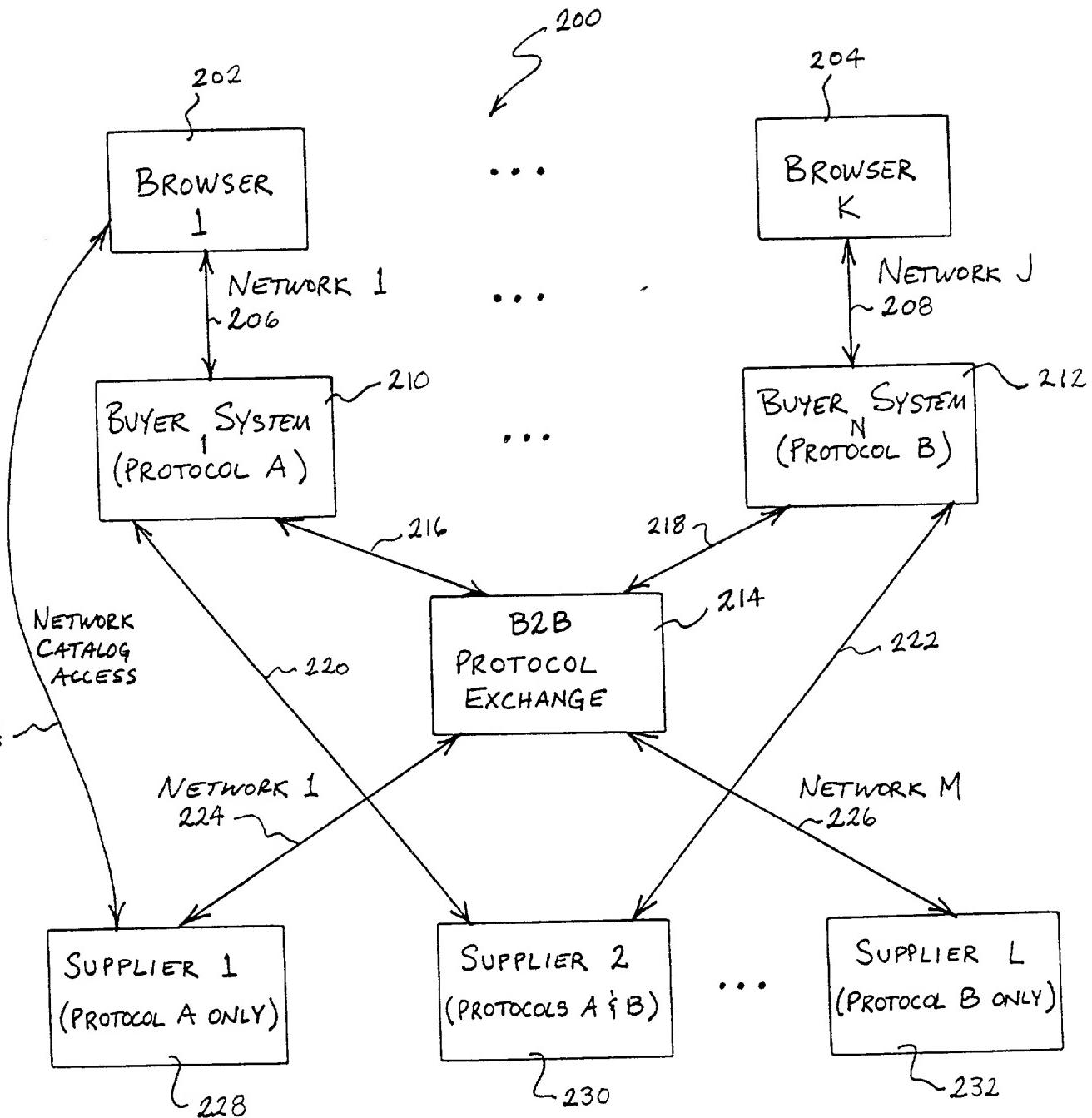


FIG. 2

3/11
YOR920010401US1

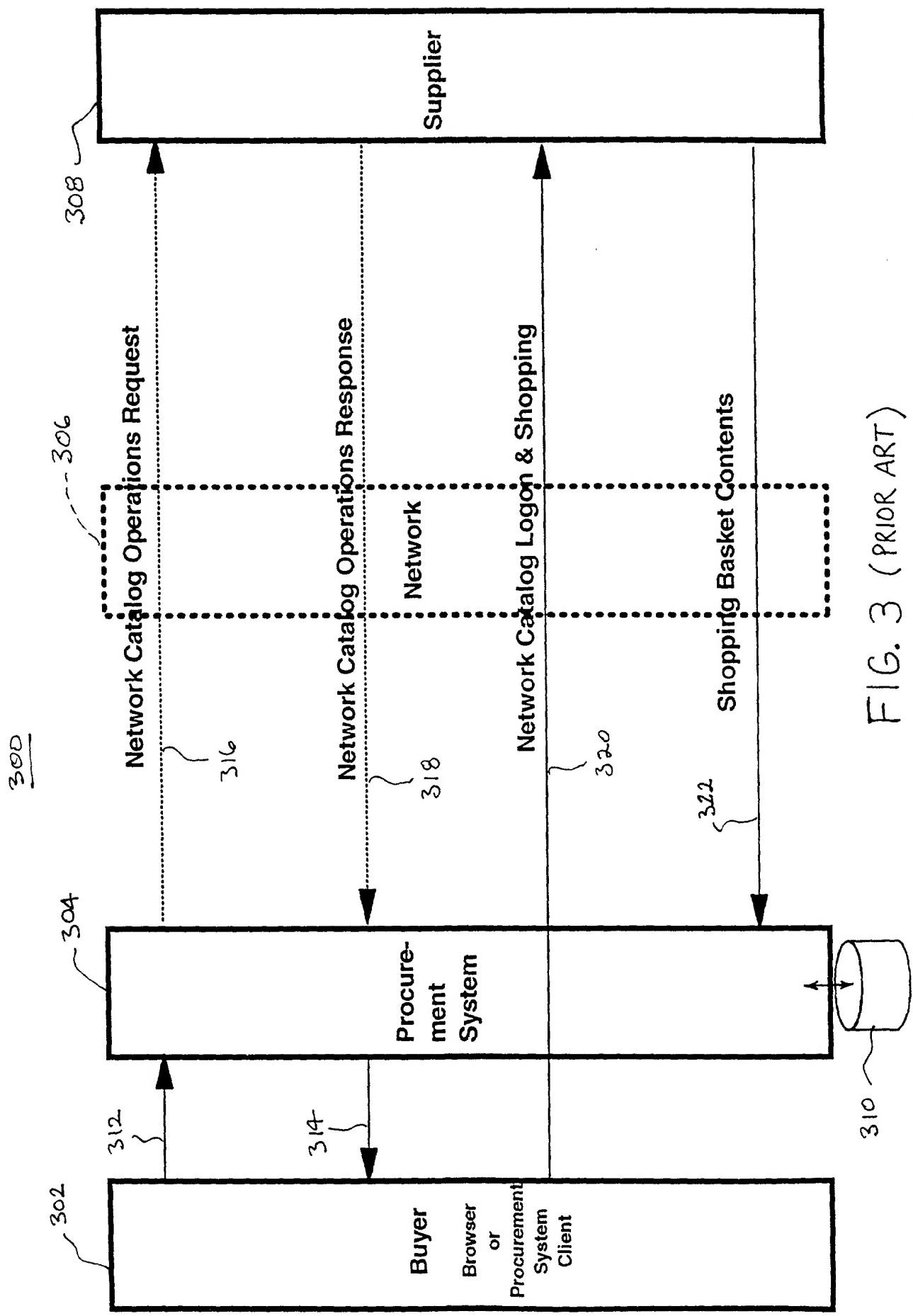


FIG. 3 (PRIOR ART)

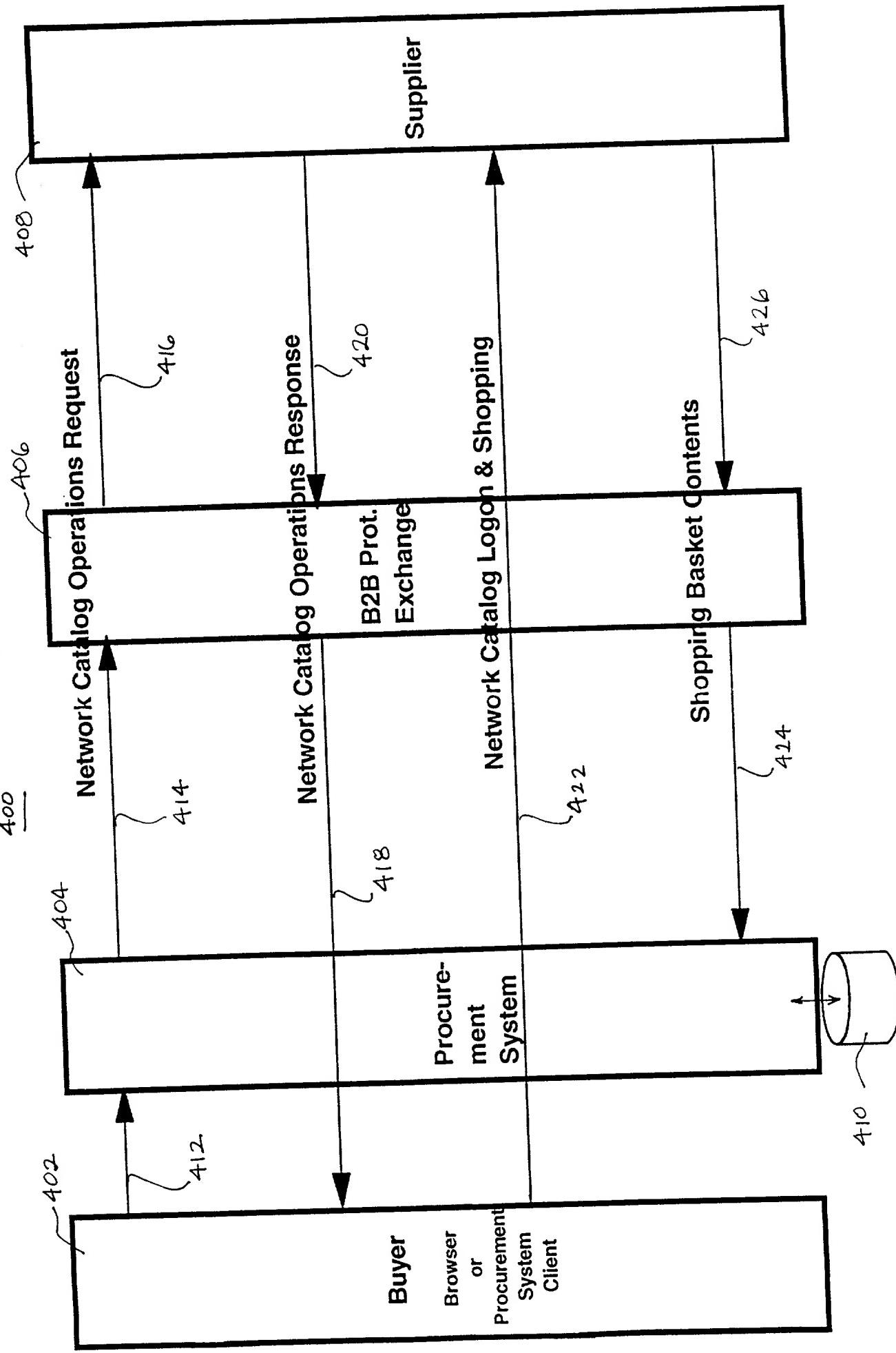
4/11
YOR920010401US1

FIG. 4

5/11
Y0R920010401US1

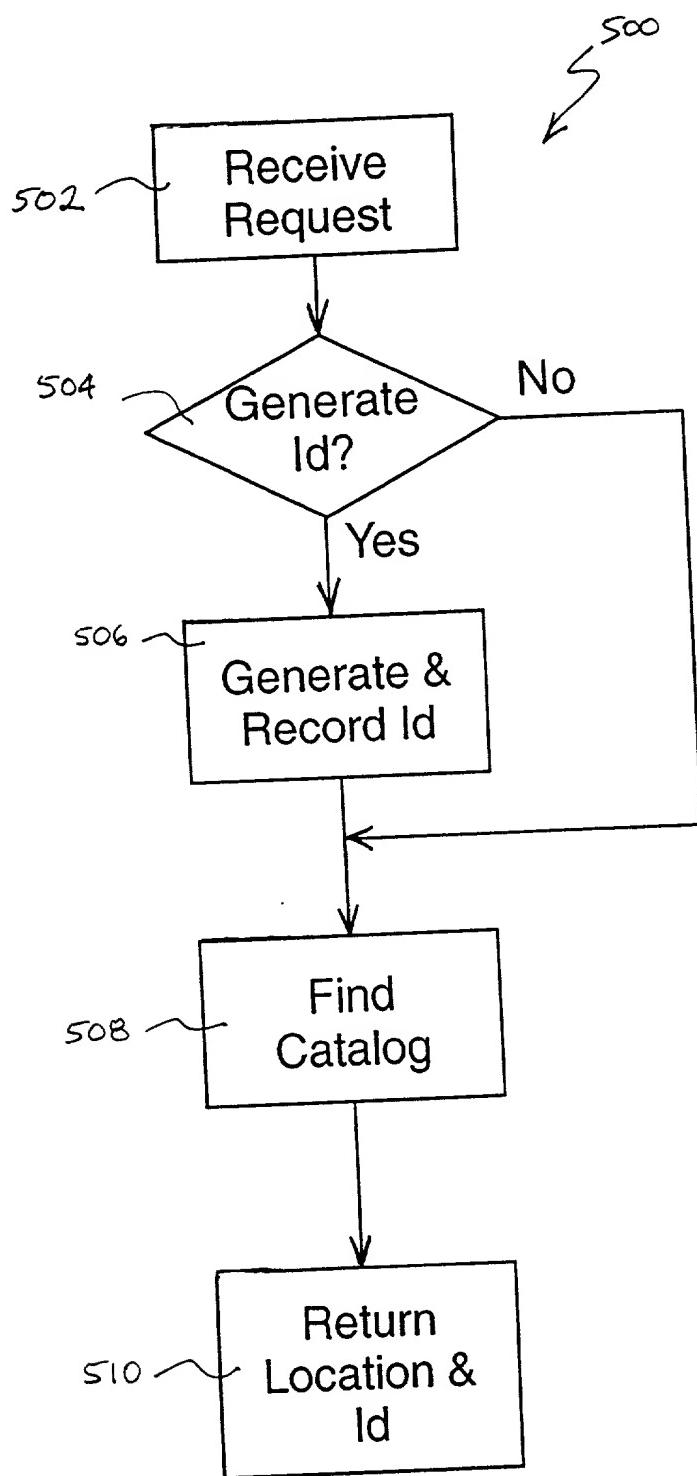


FIG. 5

6/11
YOR920010401US1

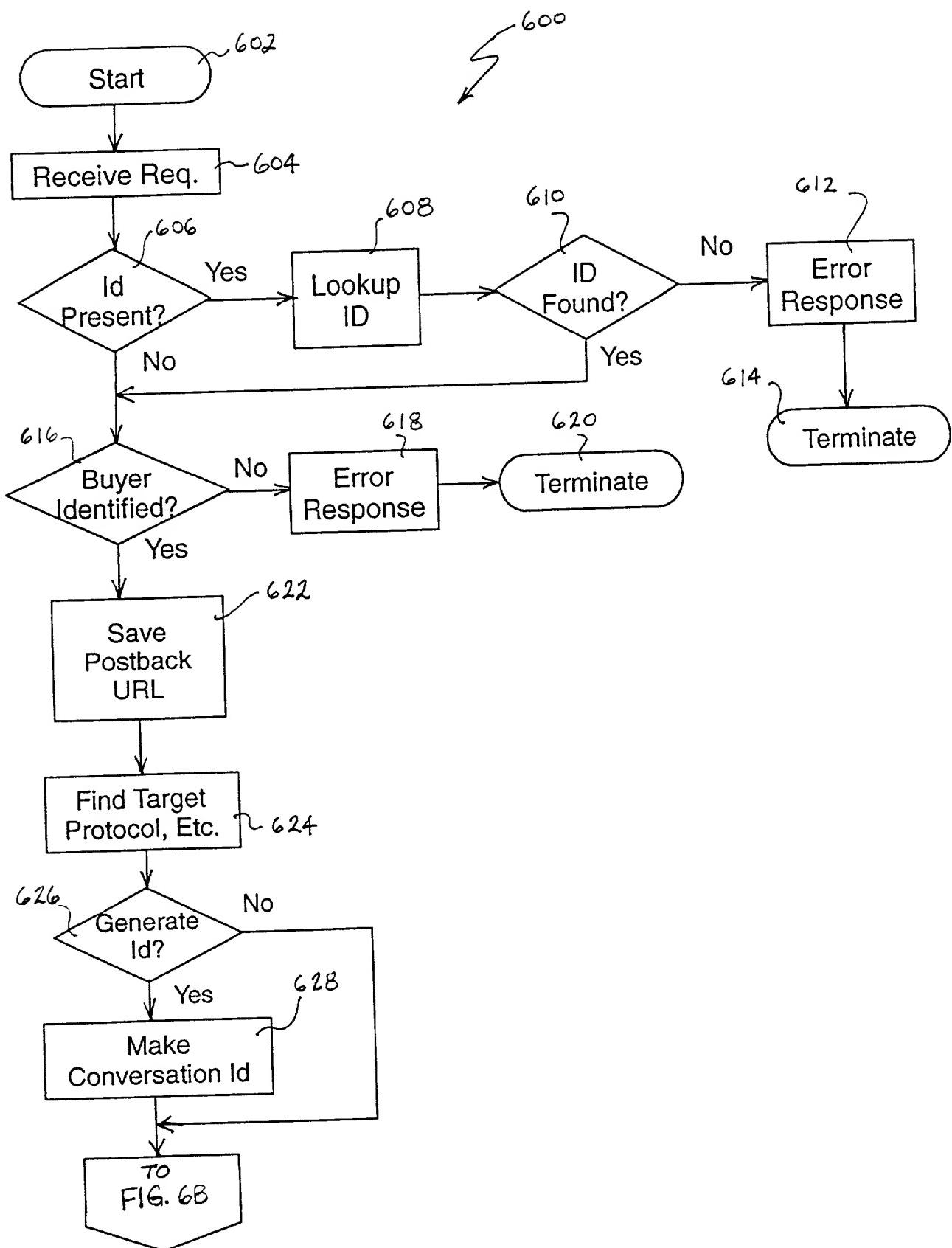


FIG. 6A

FIGURE 6A FIGURE 6B

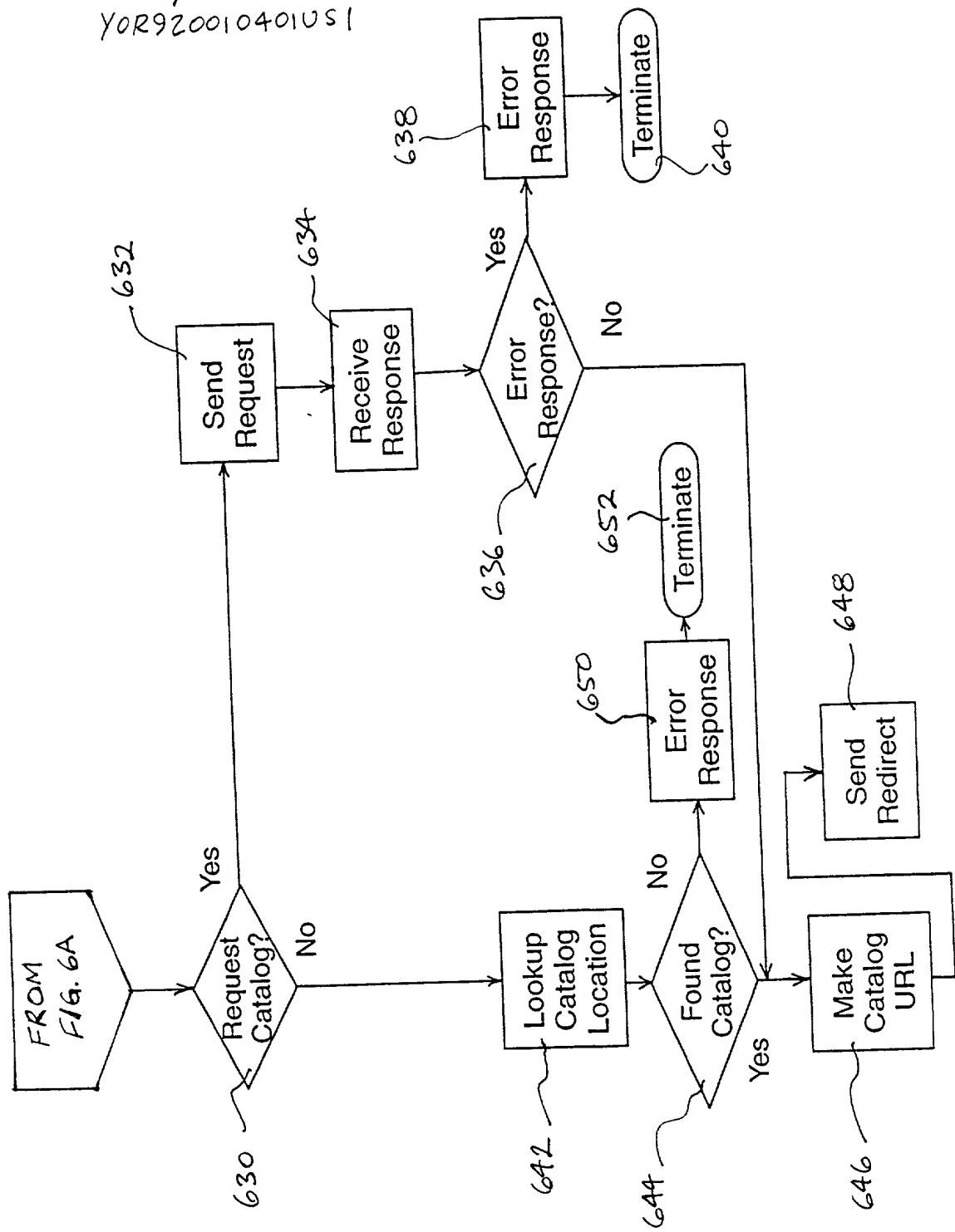


FIG. 6B

8/11

YOR920010401051

T D G a 2 0 * T 0 2 2 0 0 0 0

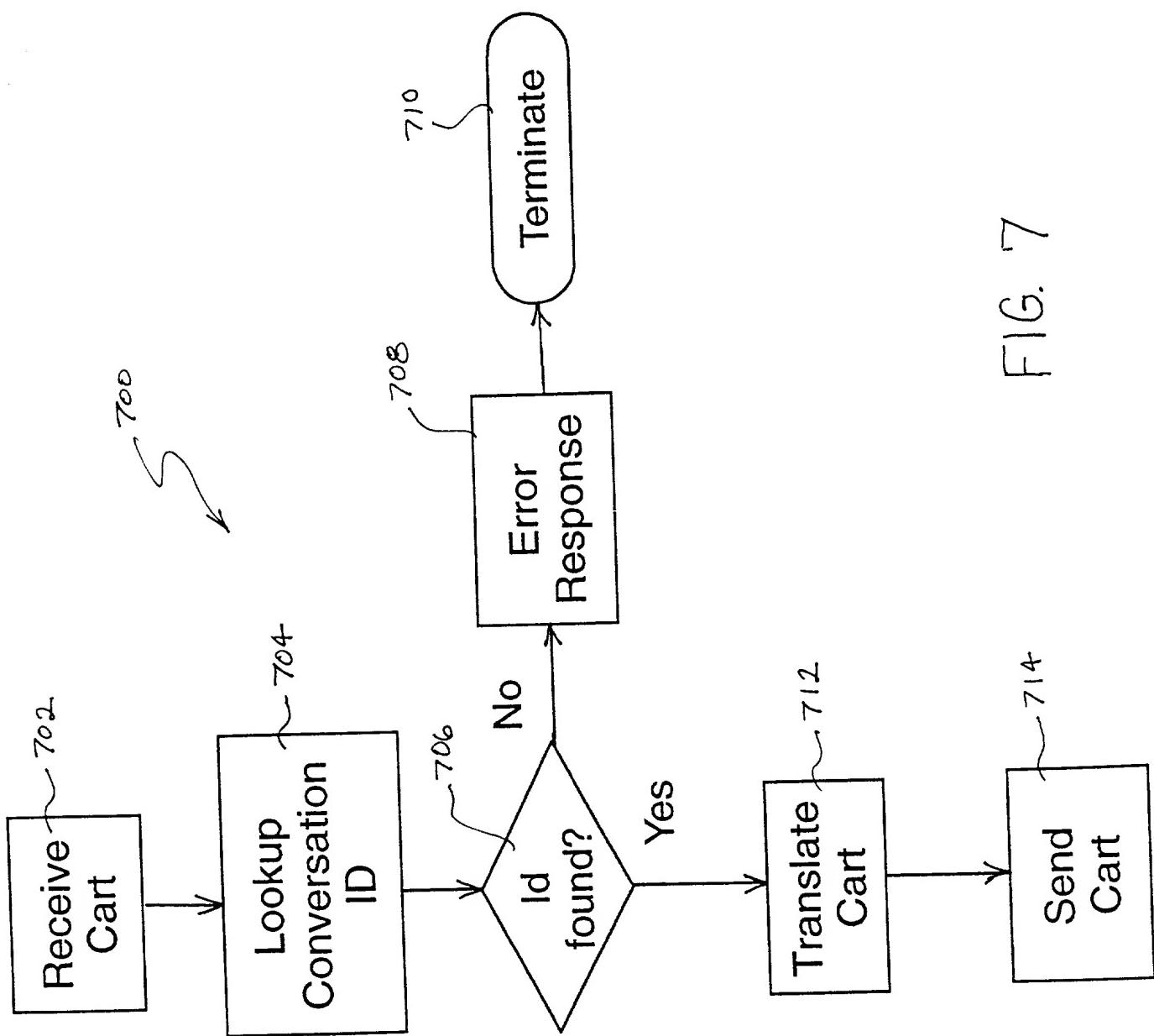


FIG. 7

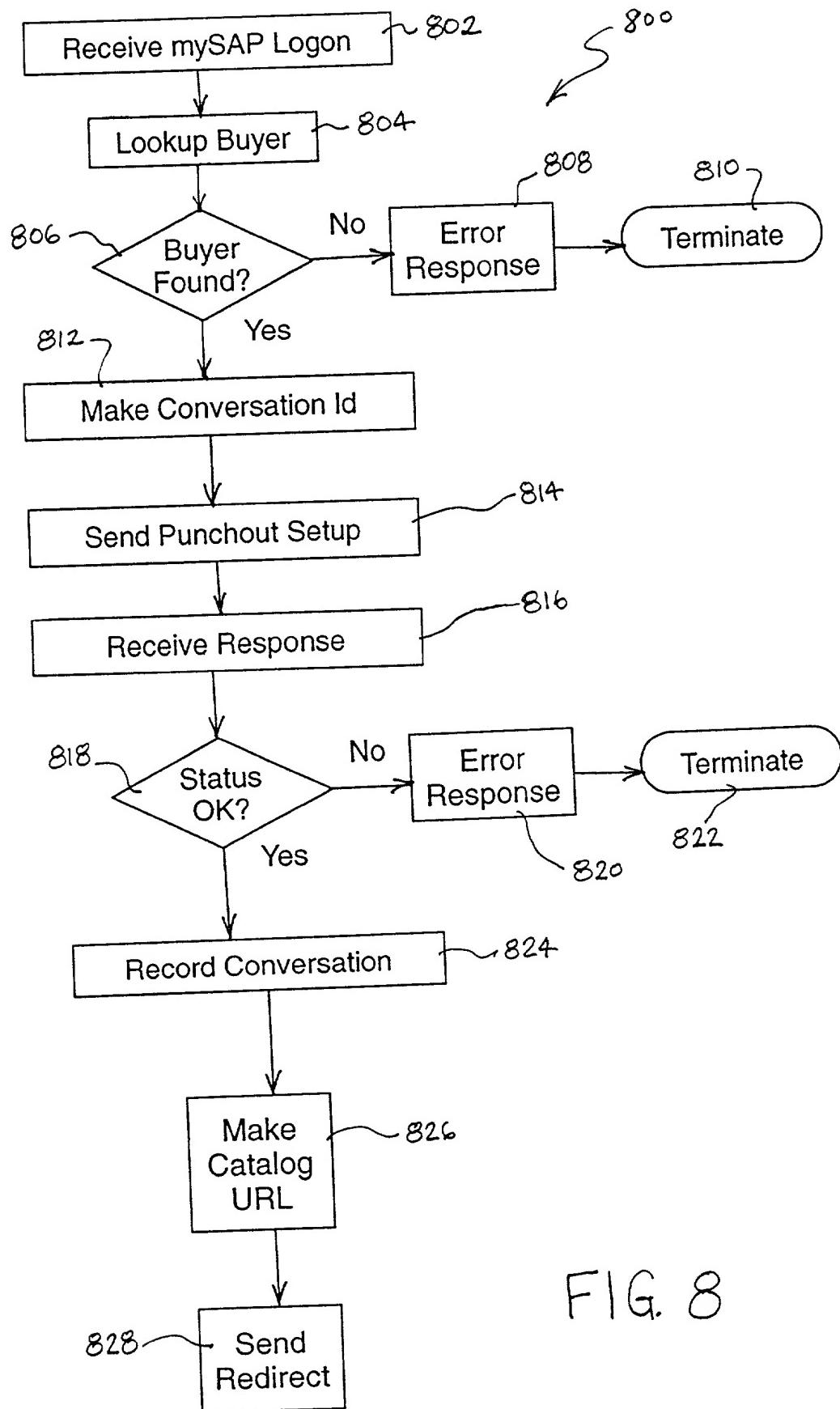


FIG. 8

10/11
YOR920010401US1

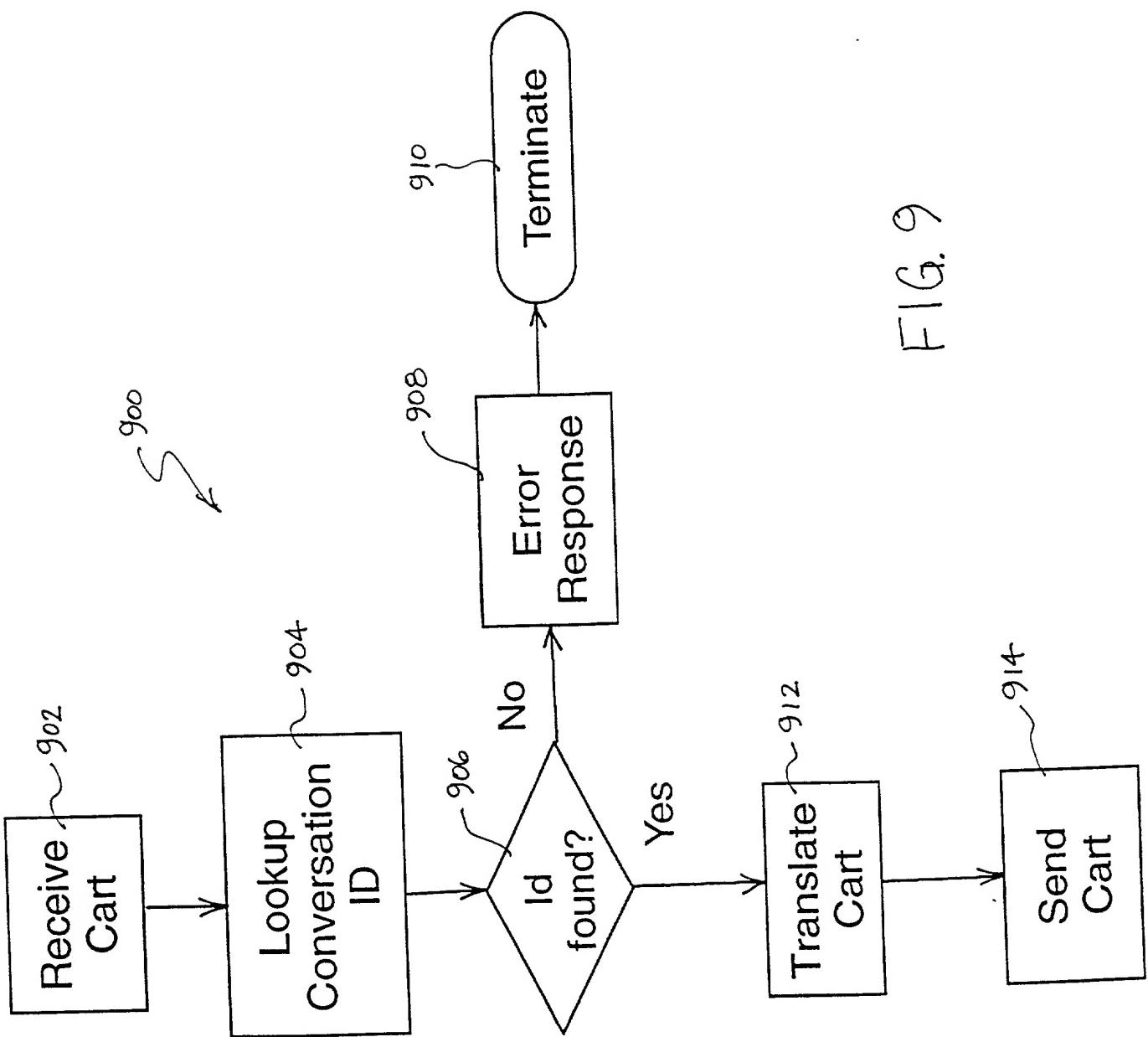


FIG. 9

11/11

Y0R920010401US1

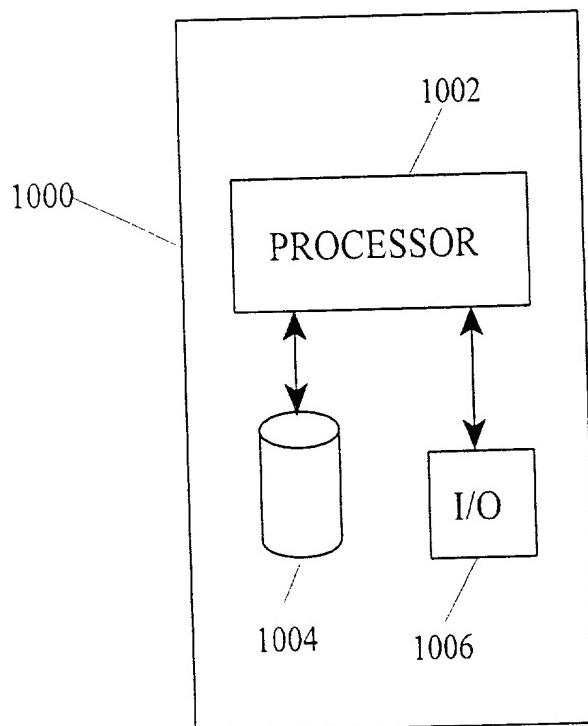


FIG. 10